amplifier, which is operated in parallel with the same optical data signal, can be regenerated with a 1/0-decision element 32 by virtue of clock recovery of that kind. For that purpose the optical 1/0-data signals are preferably encoded as return-to-zero (RZ)-signals.

Figure 12 shows a 2Q-PMD-DLL with which even higher levels of sensitivity can be achieved on the basis of an IQ-PMD-receiver, in particular with PN-modulation 11.

As in the above-mentioned patent applications to the same applicant, which form the basis for this patent application, periodic PN-modulation 11 affords great advantages in terms of PMD-reception, in particular the possibility of multi-channel selectivity, multi-target detection and the highest degree of sensitivity in respect of phase transit time resolution. In accordance with the invention it is also possible to use PN-encoded data signals for data light barrier arrangements inclusive of distance measurement and for optical CDMA-data transmission, for example, as shown in Figure 12. In that respect for example a logic '1' corresponds to a normal PN-word whereas a logic '0' corresponds to the inverted PN-word = *PN*, that is to say the light/dark chips are interchanged. In contrast to Figure 11, in Figure 12 the outputs from the summing and difference amplifier 41 are both connected to the loop filter 22 which then feeds the VCM f_{chip} 44 connected to the PN-modulation generator 11. It is the difference output voltage that is formed as the difference of the quantitative differences of the photocurrents: $U_\Delta = \text{const} \cdot (| i_a - i_b | - | i_c - i_d |)$. By means of the recovered word clock it is possible to regenerate the data signal of the PN-encoded 1/0-data sequence by a procedure whereby in the summing amplifier the sum 45 of the differences of the photocurrents $U_\Sigma = \text{const} \cdot (| i_a - i_b | + | i_c - i_d |)$ is respectively formed by way of a PN-word length by means of a short-term integrator contained in the summing amplifier 41 and in the 1/0-decision element 42 the 1/0-decision is taken in clock-synchronous manner for subsequent evaluation or regeneration.

With a VCO providing a sine modulation for the modulation 11 voltage and with the circuit element 30 where $T_{chip} = T/4$ of the sine period, it is also possible to detect and regenerate vector modulation.